REMARKS

Claims 1-20 are pending. Claims 1, 3, 8 and 9 are amended and new claims 12-20 are added. Attached is a marked-up version showing the changes to the claims made by the present amendment.

Applicants acknowledge the rejoinder of claim 8, species II. Applicants note that consideration of non-elected claim 4 will be made upon allowance of a generic claim. It should be noted that new claim 12 is a combination of the features set forth in claims 1, 3 and 7.

The Examiner has rejected claims 1-3, 5-8, 10 and 11 as being anticipated by ***Higuchi et al.*** In regard to claim 1 and its dependent claims, Applicants have amended claim 1 to include that the second channel layer is of a greater thickness than the first channel layer. ***Higuchi et al.*** does not disclose this limitation and does not derive its benefit. In ***Higuchi et al.***, the channel layer 4, In0.75ga0.25As, is 200 A, and the stress compensation layer 3, (A10.73Ga0.27)0.56In0.44As, is 50 A. A partial translation of ***Higuchi et al.*** is attached.

Contrary to amended claim 1, the stress compensation layer 3 (the second channel layer) does not have a larger thickness than the channel layer 4 (the first channel layer). Important benefits are derived from the increased thickness. As defined in claim 1, the second channel layer has an energy level of conduction band higher than that of the first channel layer and a band gap wider than that of the first channel layer. Therefore, the lower quantum level is only in the first channel layer and the higher quantum level is not only in the first channel layer but also the second channel layer. And as explained in the present specification, line 26 in page 8; line 21 in page 9; and lines 3-9 in page 21, with a higher electric field, the electron energy level becomes higher so that the electrons are mainly present at the higher energy level. Since the second channel layer is thicker than the first

channel layer, the ratio of the higher energy level electrons at the second channel layer is larger than at the first channel layer. Therefore, the impact ionization effect is significantly suppressed.

In regard to claims 10 and 11, ***Higuchi et al.*** does not disclose all the limitations of claim 10. In ***Higuchi et al.***, the channel layer 4, In0.75Ga0.25As, has a larger lattice constant than the InP substrate. Therefore, the channel layer 4 in ***Higuchi et al.*** is different from the invention of claim 10 which includes a first channel layer being lattice matched to InP. As ***Higuchi et al.*** does not teach matching lattice constants for the layers it does not anticipate the invention of claim 10 nor dependent claim 11.

The Examiner has rejected claims 1, 2 and 8 as being anticipated by ***Kohara et al.*** In ***Kohara et al.***, the channel layer 23b (corresponding to the first channel layer) has a larger band gap than the channel layer 23a (corresponding to the second channel layer). Please see Fig. 18 of ***Kohara et al.*** Since the first channel layer 23b has a smaller composition ratio of In than the second channel layer 23a, the channel layer 23b has a larger band gap than the channel layer 23a. Whereas, according to the present invention of claim 1, the first channel layer has a smaller band gap than the second channel layer. This difference is significant due to the improved function of the present invention.

In regard to claim 8, the Examiner appears to have misread the reference. The Examiner has labeled the layer, 23a the first channel layer. In fact, this layer rests on the buffer layer and therefore is the second channel layer according to claim 1. Hence, ***Kohara et al.*** discloses the opposite of the limitation of claim 8. Namely, the In composition ratio of the second channel layer is higher and the gallium composition ratio is lower than those of the first channel layer.

The Examiner has rejected claim 9 as being unpatentable over ***Higuchi et al.*** as applied to

the claims above, and further in view of Applicant's Prior Art admissions. Applicants respectfully submit that in light of the amendment to claim 1, ***Higuchi et al.*** does not disclose all necessary limitations of the base claim. As such, one skilled in the art would not derive the invention of claim 9 by combining ***Higuchi et al.*** with the admitted prior art. One skilled in the art would not ascertain that the thickness of the second channel layer must be greater than that of the first channel layer. Hence, claim 9 would not have been obvious.

With respect to new independent claim 12, support is provided at the paragraph of line 12-28 of page 16 in the present specification. That is, when the ratio of Al is 0.05-0.5, the second channel layer can be lattice matched to the first channel layer and the buffer layer, and can have the conduction level in between the first channel layer and the buffer layer. On the other hand, in ***Higuchi et al.***, the stress compensation layer 3 is (Al0.73Ga0.27)0.56In0.44As, whose ratio of Al is 0.73 lower than the new independent claim.

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosures: Version with markings to show changes made
Partial translation of ***Higuchi et al.***

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Partial Translation of Higuchi et al.

Embodiment

Fig. 2 is a cross sectional view for explaining one embodiment of the present invention, a stress compensated pseudo-morphic HEMT. In Figure, 1 is InP substrate, 2 is In0.52Al0.45As buffer layer, 3 is (Al0.73Ga0.27)0.56In0.44As stress compensated layer, 4 is In0.75Ga0.25As channel layer, 5 is In0.52Al0.48As spacer layer, 6 is n-in0.52Al0.48As carrier supply layer, 7 is In0.52Al0.48As barrier layer, 8 is In0.53Ga0.47As cap layer, 9 is a source electrode, 10 is a drain electrode, 11 is a metal composition layer, 12 is a gate electrode, and 13 is a two dimensional electron gas layer.

This embodiment is easily fabricated by employing a production technology of HEMT as employed previously.

(1) By applying MBE method, the buffer layer 2, the stress compensation layer 3, the channel layer 4, the spacer layer 5, the carrier supply layer 6, the barrier layer 7, the cap layer 8 are deposited on the substrate 1. The main data for each semiconductor layers is as follows for example.

Buffer layer 1: thickness 3000 A
Stress compensation layer 3: thickness 50 A
Channel layer 4: thickness 200 A
Spacer layer 5: thickness 50 A
Carrier supply layer 6: impurity Si, density 5×10^{18}, thickness 1000 A
Barrier layer 7: thickness 250 A
Cap layer 8: thickness 300 A

VERSION WITH MARKINGS TO SHOW CHANGES MADE
U.S. PATENT APPLICATION SERIAL NUMBER 09/981,842

IN THE CLAIMS:

Claims 1, 3, 8, and 9 have been amended as follows:

1. (Amended) A high electron mobility transistor using a Group III-V compound semiconductor, comprising

an undoped second channel layer laminated on an InP substrate via a buffer layer;

an undoped first channel layer laminated on said second channel layer; and

a doped electron-supplying layer laminated on said first channel layer,

wherein said first channel layer is composed of $In_{1-x}Ga_xAs$ and has an energy layer level of conduction band lower than that of said electron-supplying layer,

said second channel layer is composed of a Group III-V compound semiconductor using a Group V element other than P, has an energy level of conduction band higher than that of the first channel layer, [and] has a band gap wider than that of the first channel layer, and has a thickness larger than that of the first channel layer.

3. (Amended) The high electron mobility transistor as described in claim 1 [or claim 2], wherein said electron-supplying layer is composed of $In_{1-y}Al_yAs$, the first channel layer is composed of $In_{1-x}Ga_xAs$, and the second channel layer is composed of $In_{1-x}(Al_{1-z}Ga_z)_xAs$.

8. (Amended) The high electron mobility transistor as described in claim 1 [or claim 2], wherein said electron-supplying layer is composed of $In_{1-y}Al_yAs$, the first channel layer is

composed of $In_{1-x}Ga_xAs$, and the second channel layer is composed of $In_{1-x}Ga_xAs$ with the In composition ratio lower and the gallium composition ratio higher than those in the first channel layer.

9. (Amended) The high electron mobility transistor as described in claim 1 [or claim 2], wherein an element separation groove is formed which extends from said electron-supplying layer to said buffer layer.